7E7086

Roll No. 15EEBEC021 Total No of Pages: 3

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B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. – 2018
Electronics & Communication Engineering
7EC6.3A VHDL

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Describe the programming structure of VHDL and also explain Functional Simulation. [8]

(b) Describe the Behavioral & Structural style of modeling with suitable example. [8]

OR

Q.1 Write a VHDL code for -

(a) D – Latch. [4]

(b) Half adder [4]

(c) 4 × 1 MUX [4]

(d) 3 - input NAND gate [4]

UNIT- II

Q.2 (a) Explain Sequential statements with example. [8]

(b) VHDL Description of structure with suitable example? [8]

OR

Q.2 (a) Given the following function f = ab + cd. Write an entity declaration and alternative architectures for a system that computes the function. [8]

(b) Explain Model Organization with example. [4]

(c) What is NULL Transactions? Explain. [4]

UNIT- III

Q.3 (a) Consider the function: $y = \overline{x_1}\,\overline{x_3} + x_2\,\overline{x_3} + \overline{x_1}\,x_2$. Use the truth table to derive a circuit for y that uses a 2 – to – 1 MUX. [8]

(b) Write a VHDL Code that specifies the barrel shifter circuit. [8]

OR

Q.3 (a) Explain in brief Binary encoder & Binary decoder and explain Sensitivity list. [8]

(b) Write a VHDL Code for a BCD – to – 7 Segment Code converter using a select signal assignment. [8]

UNIT- IV

Q.4 (a) Write a VHDL Code of Serial Adder and also explain one hot encoding. [8]

(b) Write short note on Mealy type FSM with example. [8]

OR

Q.4 (a) Write down short note on Vending Machine with example. [8]

(b) Write down VHDL Code for Moore type FSM and also be explain Mealy type finite state machine. [8]

UNIT- V

Q.5 (a) How many 16K memories can be placed (without over lapping) in the memory space of a processor that has 24 address lines? [8]

(b) Using Logic gates, design an active low chip select for the memory device described in each of the following situations. [8]

OR

Q.5 (a) Explain SRAM in brief and what is Clock skew and how it can be minimized? [8]

(b) Write a VHDL Code for Sorting operation and Multiplier. [8]
